**Instantiate Clock IP**

1. Find the core:

* Click on IP Catalog in the Project Manager area,
* Type the name of the core you are looking for in the search bar. In our case “clock”
* Click on the Clocking Wizard



2. Configure the IP core:

* Change the Primary frequency to 50Mhz



* Set clk\_out1 to 74.25Mhz
* Set clk\_out2 to 371.25Mhz
* Set reset to active low (off screen at bottom)
* Select locked (off screen at bottom)
* Ignore WARNING text
* Click OK



In the Generate Output Products pop-up, click Generate



In the Generate Output Products pop-up, click OK



Add the clk\_wiz\_0 component to your package file as follows:

component clk\_wiz\_0 is

 PORT (

 clk\_out1 : OUT STD\_LOGIC;

 clk\_out2 : OUT STD\_LOGIC;

 resetn : IN STD\_LOGIC;

 locked : OUT STD\_LOGIC;

 clk\_in1 : IN STD\_LOGIC);

end component;

**Install Custom IP core for HDMI**

1. Download the provided IP core found at

https://www.realdigital.org/doc/715356000ec89fbfd26a44cd2444659b



1. Unzip the contents of this and place the resulting folder (RD\_hdmi\_ip2020) in a folder called <course>/LabAssignments/ipRepo You will be building IP later in the course and will store it in this same folder.
2. Add the repository:
* Click IP Catalog
* Right mouse click Vivado Repository
* Select Add Repository…



1. In the pop-up, navigate to the ipRepo folder, click select. Click OK in the Add Repository pop-up.
2. If you’ve added IP to the ipRepo folder after that already having added it, then you will want to select Refresh All Repositories instead of Add Repository…

**Instantiate RGB to HDMI Converter**

1. Double click the HDMI/DVI Encoder from User Repository



1. In the Customize IP pop-up, set the Mode to HDMI. Click OK.



1. In the Generate Output Products pop-up, click Generate.



1. Click OK in the Generate Ouput Products pop-up.



1. You should now have



1. You can see the details of the interface by opening hdmi\_tx\_0.v Yes, this is a Verilog file and the Vivado tool can compile together HDL files that are written in Verilog and VHDL.

